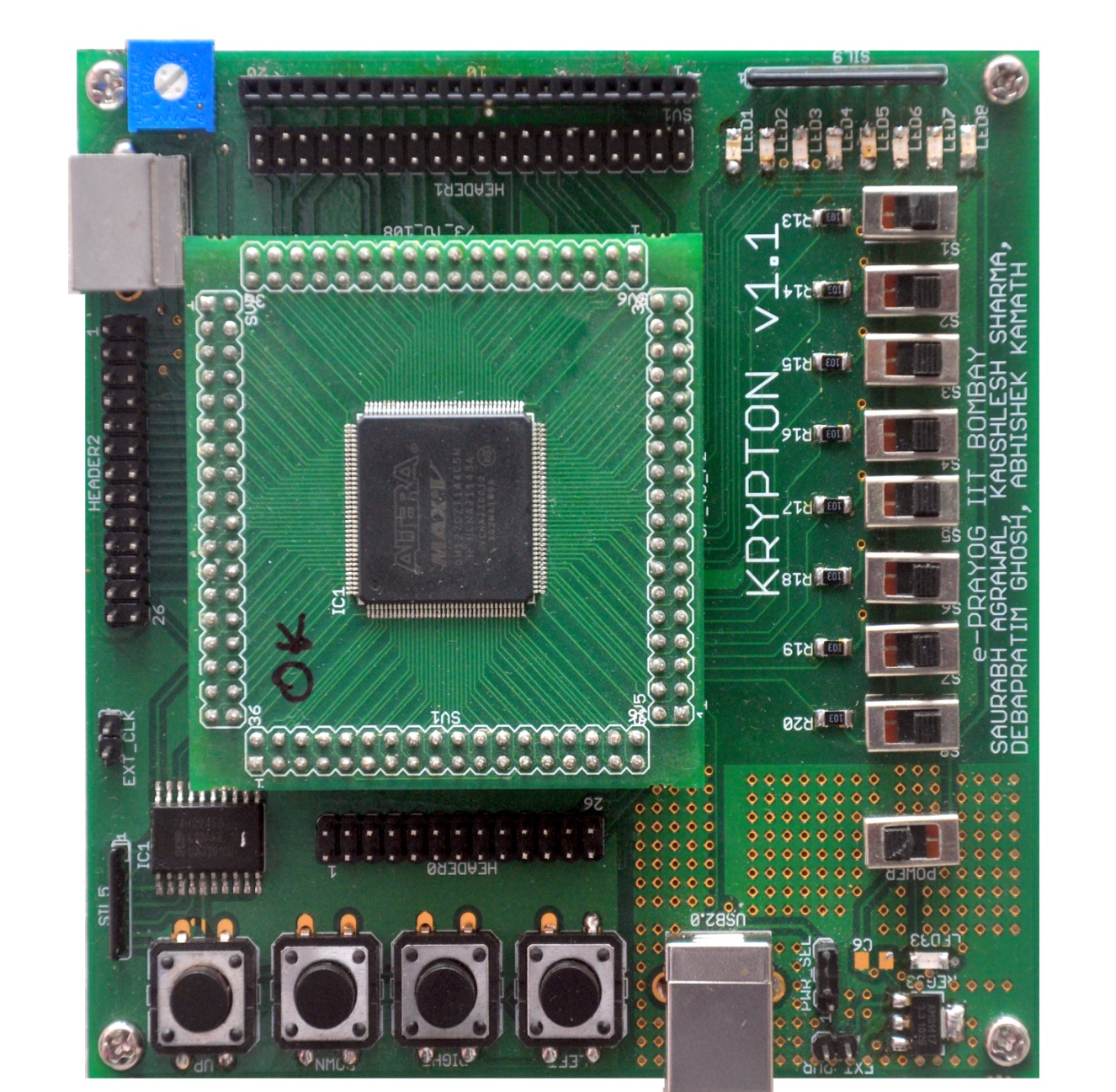
**KRYPTON v1.2 USER MANUAL**

e-PRAYOG, IIT Bombay

(Wadhwani Electronics Lab)

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**Chapter 1: About Krypton**

Krypton v1.1 (hereafter referred to as Krypton) is a 5M1270ZT144C5N CPLD-based board developed at e-Prayog, WEL Lab, IIT Bombay under the Virtual Labs Project by the Ministry of Human Resource and Development (MHRD), Government of India. This is a low-cost solution aimed to cater to the needs of undergraduate and graduate electrical/electronics engineering students in a course in digital design and thereafter, design of fairly complex digital systems.

Krypton is currently designed for CPLDs from Altera MAX V and can also support MAX II family devices, Cyclone IV FPGA family devices and also Spartan 6 FPGA family devices. All the above family devices have been tested successfully. This feature of Krypton makes it very useful as the platform can be used as a programmer for many devices and also for development of customized applications where on board peripherals are not used. The modular design of Krypton facilitates the use of CPLD module for much ambitious and complex project development. The Top module which is Hot-Socketed consist of a 144 pin TQFP integrated circuit of which the pins are routed systematically to the edges making it easy to use for other customized application. Second it consists of a 50MHz crystal oscillator soldered on the bottom surface of the PCB which can be easily changes according to developers needs. Third it consists of 2 power indicator LED indicating proper power supply to the device.

Krypton as a whole consists of some very useful peripherals and connectors that can be used for project development by the beginners and intermediate level students and hobbyist. For the development complex projects CPLD hot-socketed module can be used with customized platform. Further a brief introduction of all the peripheral is given which will be discussed in greater detail.

**Board Features and specifications:**

* Device independence: supports Altera MAX V, MAX II, Cyclone IV, and Xilinx Spartan 6 any JTAG compatible device
* Device used in Krypton v1.2: 5M1270ZT144C5N (refer Device Handbook(1) for more details)
* Powered and Programmed through USB with facility to be powered externally
* 8 inputs switches
* 8 outputs LEDs
* 86 programmable GPIOs
* Onboard clock of 1Hz generated using 555 timer as a astable multivibrator
* 50 MHz crystal oscillator
* External clock input
* 4 buffered push buttons with hardware de-bounce
* PS2 connector for Mouse/Keyboard interface
* LCD/GLCD connector

**Important Notes:**

* Do not touch any IC with your hands as they may be damaged due to electrostatic discharge, moisture etc.
* When using an external supply to power the board, use only a single regulated +5V DC supply
* All input voltage levels must be 3.3v
* Use external power supply for application utilizing high power
* When using external power supply change the power select jumper position
* Carefully attach detach Hot-socketed module, GLCD/LCD module
* Interfacing to be done only when power is off
* Improper connections may short power points which will damage the board

**Chapter 2: Installations and Getting started**

**Installing the Drivers:**

**For Windows:**

1. Extract the krypton related material to any directory.
2. Plug Krypton to a PC with Windows/Linux via USB and switch on the power, red LED should glow on both Mother and hot-socketed daughter board (a total of 3 LED glows 2 with same brightness and 1 slightly less bright).
3. The **“Found new hardware”**, wizard should open, if new hardware wizard doesn’t pops up the go to devices manager and install the device driver from there.
4. Select **“No, not this time”** and click **next**
5. Select **“Install from a specific location”**, and click **next**.
6. Navigate to the folder containing the CDM20817 drivers in Krypton related material folder extracted in step 1 and click **OK**. Then click **continue anyway.**
7. The drivers will be installed after the same process is repeated 4 times i.e. for Serial Converter A, B, and twice for the two serial ports.
8. Install urJTAG from jtag.exe provided in the krypton related material folder.

It is recommended that you keep a copy of the drivers and materials in your computer. You may need to install the drivers again if a different board is connected. Refer to troubleshooting guide if you find any difficulty installing and/or using urJTAG also refer to our YouTube channel for video tutorials on **Installing the driver and urJTAG(windows)**.

**For Linux:**

1. Untar **libftd2xx1.1.12**
2. In terminal, type **sudo nautilus, i**n nautilus navigate to the folder in which you have extracted **libftd2xx1.1.12 and copy** **ftd2xx.h** and **Wintype.h** in this folder into **/usr/local/include/**
3. Go to **release/build/x86\_64 and c**opy **libftd2xx.so.1.**1 and paste in **/usr/local/lib/**
4. In terminal, type the following

* **chmod 0755 /usr/local/lib/libftd2xx.so.1.1.12**
* **ln -sf /usr/local/lib/libftd2xx.so.1.1.12 /usr/local/lib/libftd2xx.so**

1. Untar urjtag-0.10.tar.gz and go to that folder
2. In terminal, type

* **./configure**
* **make**
* **sudo make install**

1. To make sure if the libraries are install properly, after **./configure**, there should be a yes after **libftd2xx** i.e. **Detected libftd2xx : yes**
2. In terminal, type **export LD\_LIBRARY\_PATH=/usr/local/lib**
3. Remove unwanted modules by typing in terminal

* **lsmod**
* **rmmod ftdi\_sio**
* **rmmod usbserial**

1. Install cable drivers by Copying  **“99-libftdi.rules”** to **/etc/udev/rules.d**
2. type **jtag** in terminal

It is recommended that you keep a copy of the drivers and materials in your computer. You may need to install the drivers again if a different board is connected. Refer to troubleshooting guide if you find any difficulty installing and/or using urJTAG also refer to our YouTube channel for video tutorials on **Installing the driver and urJTAG(Linux)**.

**Installing and getting started with Altera Quartus:**

1. Install the latest version of Altera Quartus web edition from Altera’s website. Refer link at (2)
2. Open Quartus, **New project wizard** should open, click **Create a new project.** If new project wizard doesn’t open from **File » New Project Wizard**. Click **next**
3. Create a working directory with short path address for e.g. c:\ MyProject. Next the project name and the top level design entity should have the same name and which is case sensitive. Provide any name with no spaces for e.g. MyDesign
4. An existing VHDL/Verilog file can be added to the project if a design has been already made else it may be left blank if you wish to create new VHDL/Verilog design in the current project directory. Click **next**.
5. Select the programmable device family as MAX V, and 5M1270ZT144C5N from the device list that shows up. Click **next**.
6. In the EDA tools settings page you can select different EDA tools after you have installed an authentic tool version. If you are a beginner you can skip and click **next** else feel free to Google and use the tools in your design.
7. Open a new VHDL/Verilog design file from **File » New** and make the hardware design using the respective HDL.
8. After design is complete compile the design by clicking on **Start Compilation.** Shortcut **ctrl + L**
9. Once the design is compiled, you make the pins assignments as from **Pin Planner** under the Assignments tab in the Menu bar. Shortcut **ctrl + shift + N.** Refer this document for pin configuration and planning.
10. After making the pin assignments compile the design again for the change to take affect.
11. Now generate programming file .svf file. To generate the **.svf** file, select **Tools » Programmer**.
12. Go to File **» Generate JAM, JBC, SVF or ISC file.** Then select **Serial Vector Format (SVF)** in file type and click ‘Generate’. This will create a .svf file in the working directory selected during the creation of new project. Refer to our YouTube channel for video tutorials on **Using Quartus and generating programming files**.

For more information and updates (if any) on using Quartus and new hardware peripherals and driver updates refer to the Virtual Lab website.

**Note:** The complete process from creating the project, defining Top-level entity, selecting the appropriate device, compiling your design, making pin assignments (dedicated to Krypton) and then at least creating the svf file can be automated using TCL scripting. Will be explained in later.

**Programming the MAX V CPLD:**

1. Open the JTAG shell in the UrJTAG folder in windows and type **jtag** in Linux terminal.
2. At the jtag prompt, type **cable ft2232**.
3. You will get a message saying **connected to libd2xx**.
4. Then type **detect,** this will identify the CPLD device and display its signature and device ID etc.
5. In case you have other devices connected to the JTAG chain, you can choose the appropriate device by specifying the corresponding part number. This is optional in this case, as only one device is present in the JTAG chain. Since the CPLD is the only device in the JTAG chain, you can select it by typing the part 0 command.
6. Next type **svf svf\_file\_location/filename.svf** or **svf svf\_file\_location/filename.svf progress stop** on the command prompt. The file will now configure the device.

For the complete reference of installation and setting up the hardware please go to **Getting started with Krypton** video tutorial on our YouTube Channel.

PUSH BUTTON

**Chapter 3: Pin Assignments for On-Board Peripherals**

To make the Pin assignments in Quartus go to Assignments >> Pin Planner or Ctrl + Shift + ‘N’. While making the assignments the following information will be required very often.

1. Using the Switches.

|  |  |
| --- | --- |
| **Switch** | **Pin No.** |
| S1 | 48 |
| S2 | 45 |
| S3 | 44 |
| S4 | 43 |
| S5 | 42 |
| S6 | 41 |
| S7 | 40 |
| S8 | 39 |

1. Using the LEDs

|  |  |
| --- | --- |
| **LED** | **Pin No.** |
| LED-1 | 58 |
| LED-2 | 57 |
| LED-3 | 55 |
| LED-4 | 53 |
| LED-5 | 52 |
| LED-6 | 51 |
| LED-7 | 50 |
| LED-8 | 49 |

1. Using the Push Button Switches

|  |  |
| --- | --- |
| **Push Button** | **Pin No.** |
| Up | 141 |
| Down | 142 |
| Right | 143 |
| Left | 144 |

1. On-Board Clock

|  |  |
| --- | --- |
| **Frequency** | **Pin No.** |
| External | 91 |
| 50 MHz | 89 |
| 1 Hz | 18 |

1. PS2 connector of Mouse and keyboard interface

|  |  |
| --- | --- |
| **Pin Name** | **Pin No.** |
| Data | 140 |
| Clock | 139 |

1. GLCD/LCD shared connector

|  |  |  |
| --- | --- | --- |
| **GLCD/LCD Pin No.** | Pin Name | Krypton Pin No. |
| 1 | GND | Ground |
| 2 | VDD | Vcc = +5 V |
| 3 | V0 | GLCD output = -10 V |
| 4 | RS or DS | 70 |
| 5 | R/W | 72 |
| 6 | E | 74 |
| 7 | D0 | 76 |
| 8 | D1 | 80 |
| 9 | D2 | 84 |
| 10 | D3 | 86 |
| 11 | D4 | 88 |
| 12 | D5 | 94 |
| 13 | D6 | 96 |
| 14 | D7 | 98 |
| 15 | CS1 | 102 |
| 16 | CS2 | 104 |
| 17 | RESET | 106 |
| 18 | VOUT | Contrast |
| 19 | LED+ | Vcc = + 5 V |
| 20 | LED- | Ground |

1. GPIO Headers for other peripheral interfacing

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Header 0** | | **Header 1** | | **Header 2** | |
| 1 | 2 | 59 | 62 | 109 | 110 |
| 3 | 4 | 63 | 66 | 111 | 112 |
| 5 | 6 | 67 | 68 | 113 | 114 |
| 7 | 12 | 69 | 70 | 117 | 118 |
| 13 | 14 | 71 | 72 | 119 | 120 |
| 15 | 16 | 73 | 74 | 121 | 122 |
| 21 | 22 | 75 | 76 | 123 | 124 |
| 23 | 24 | 77 | 80 | 126 | 130 |
| 27 | 28 | 79 | 84 | 127 | 132 |
| 29 | 30 | 81 | 86 | 129 | 134 |
| 31 | 32 | 85 | 88 | 131 | 138 |
| 37 | 38 | 87 | 94 | 133 | 139 |
| Gnd | Vcc | 89 | 96 | Gnd | Vcc |
|  |  | 93 | 98 |  |  |
|  |  | 95 | 102 |  |  |
|  |  | 97 | 104 |  |  |
|  |  | 101 | 106 |  |  |
|  |  | 103 | 107 |  |  |
|  |  | 105 | 108 |  |  |
|  |  | Gnd | Vcc |  |  |

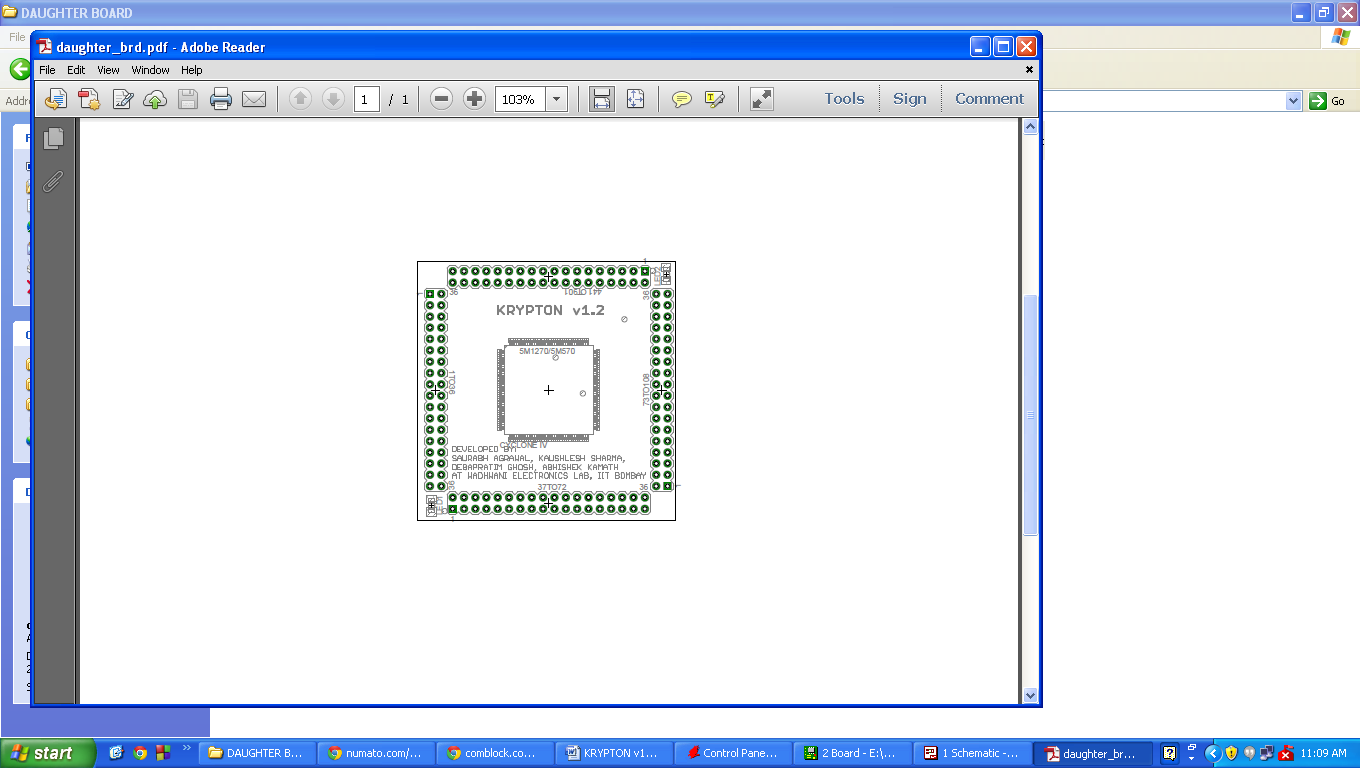
1. Hot – Scocket on the main board for MAX – V (5M1270ZT144C5N): each side of the TQFP 144 pin package has 36 pins. The table below will help you to make your PCB design to use this hot-socket in your application. The table has 4 main columns each divided in half the top left of each main column is the pin 1 as marked on the MAX-V hot socket. Read the MAX-V data sheet for details information of the device.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin 1 – Pin 36** | | **Pin 37 – Pin 72** | | **Pin 73 – Pin 108** | | **Pin 109 – Pin 144** | |
| I/O 1 | I/O 2 | I/O 37 | I/O 38 | I/O 73 | I/O 74 | I/O 109 | I/O 110 |
| I/O 3 | I/O 4 | I/O 39 | I/O 40 | I/O 75 | I/O 76 | I/O 111 | I/O 112 |
| I/O 5 | I/O 6 | I/O 41 | I/O 42 | I/O 77 | **GND** | I/O 113 | I/O 114 |
| **3.3 V** | I/O 8 | I/O 43 | I/O 44 | I/O 79 | I/O 80 | **GND** | **3.3 V** |
| **GND** | **GND** | I/O 45 | **3.3 V** | I/O 81 | I/O 82 | I/O 117 | I/O 118 |
| I/O 11 | I/O 12 | **GND** | I/O 48 | **GND** | I/O 84 | I/O 119 | I/O 120 |
| I/O 13 | I/O 14 | I/O 49 | I/O 50 | I/O 85 | I/O 86 | I/O 121 | I/O 122 |
| I/O 15 | I/O 16 | I/O 51 | I/O 52 | I/O 87 | I/O 88 | I/O 123 | **GND** |
| **GND** | I/O 18 | I/O 53 | **GND** | I/O 89 | **2.5 V** | I/O 125 | **2.5 V** |
| 2.5 V | **GND** | I/O 55 | **2.5 V** | I/O 91 | **GND** | I/O 127 | I/O 128 |
| I/O 21 | I/O 22 | I/O 57 | I/O 58 | I/O 93 | I/O 94 | I/O 129 | I/O 130 |
| I/O 23 | I/O 24 | I/O 59 | I/O 60 | I/O 95 | I/O 96 | I/O 131 | I/O 132 |
| **3.3 V** | **GND** | I/O 61 | I/O 62 | I/O 97 | I/O 98 | I/O 133 | I/O 134 |
| I/O 27 | I/O 28 | I/O 63 | **3.3 V** | **GND** | **3.3 V** | **GND** | **3.3 V** |
| I/O 29 | I/O 30 | **GND** | I/O 66 | I/O 101 | I/O 102 | I/O 137 | I/O 138 |
| I/O 31 | I/O 32 | I/O 67 | I/O 68 | I/O 103 | I/O 104 | I/O 139 | I/O 140 |
| I/O 33 | I/O 34 | I/O 69 | I/O 70 | I/O 105 | I/O 106 | I/O 141 | I/O 142 |
| I/O 35 | I/O 36 | I/O 71 | I/O 72 | I/O 107 | I/O 108 | I/O 143 | I/O 144 |

**Chapter 4: Automation of the Process**

Once you have understood the complete process completely and thoroughly well. The procedure can be automated to save time and effort. All that is required is to install TCL script. There are many more practical advantages of scripting which one can encounter by using scripts with more intelligence. A sample script is given below. To use this script you should name all the I/O pins according the pins description in Chapter 2. For details on TCL scripting use the TCL scripting manual ().

**Chapter 5: Mechanical Specification**

 To design customized design using MAX V CPLD daughter board the essential measurements for designing PCB are as shown below. The center to center spacing between two pins is 2.54 mm or 100mil, center to center distance between parallel connectors is 50.8 mm or 2000 mil. Please make sure to use the exact sizes for development of PCB. To make sure the sizes match take a print out on a plane paper with no scaling (scaling factor 1) of your design and place the daughter board over the print, each pin should match exactly with each other. Please refer to hot-socketing information in chapter 3 point 8 for the pin description. Please notice two LEDs at bottom left and top right corner which represent 3.3v and 1.8v respectively. All the power and Ground pin have already been connected so connecting 3.3v, 1.8v and ground to any one pin will connect all to voltage and ground pin, but it is recommended to connect all pins with their required voltage levels to avoid localized heating at some particular pin due to current sourcing and sinking.

100 mil or 2.54 mm

2000 mil or 50.8 mm

2000 mil or 50.8 mm

Links for downloading software:

1. http://www.altera.com/download/software/quartus ii we (Download the Web Edition v10.1 or later. You may be required to register on the website.)

2. http://urjtag.org (It is available free!! No registration required.) Install urJTAG from the above link and then replace the installed folder in program file with the folder provided in the zip file.

For any queries or support contact: cpld.wel@gmail.com